# Pipeline Adder

## Block Diagram

Diagram, schematic

Description automatically generated

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## Propagation Time Estimation

## Time Taken to add 4 pairs of numbers

// we used 8-bit ripple adders.

## Verilog Code

---*code snap---*

## Simulation Result

A picture containing timeline

Description automatically generated

As you can see, after 3rd clock cycles, result of first pair is available in the S register. After 4th clock cycles, result of second pair, after 5th clock cycles, result of third pair, and after 6th clock cycles, result of fourth pair are available in the S register.